

Remarks:

Reconsideration of the application is requested.

Claims 1-6 and 16-25 remain in the application. Claim 16 has been amended. Claims 1-6 have been withdrawn from consideration.

In item 1 on page 2 of the above-identified *Advisory Action*, the Examiner stated that the proposed amendment to claim 19 correcting the claim dependency was not entered because it would raise a new issue requiring further search and consideration. In the attached *Request for Continued Examination* (RCE) the Examiner is requested to enter the amendments proposed in the previous response. These amendments will also correct the informality in the claim dependency of claim 21.

In item 4 on page 2 of the *Advisory Action*, the Examiner maintained the rejection of claims 16-20 and 24 as being obvious over by *Hsu* (US 5,468,657) in view of *Sato et al.* (US 6,121,117) under 35 U.S.C. § 103.

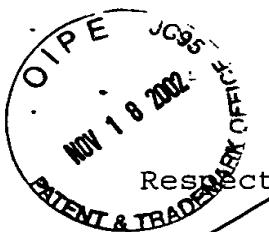
The detailed comments by the Examiner in the second paragraph on page 3 of the *Advisory Action* have been carefully noted by Applicants. Claim 16 has been accordingly amendment in view

of the Examiner comments. Support for the changes is found in the paragraph bridging pages 15-16 of the specification.

In view of the arguments brought forth in the previous responses, the Examiner's comments in the *Advisory Action*, and the subsequent amendment of claim 16, it is believed to be clear that *Hsu* in view of *Sato et al.* do not suggest the features of claim 16. Claim 16 is, therefore, believed to be patentable over the art and since claims 17-25 are ultimately dependent on claim 16, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 16-25 are solicited.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.



Respectfully submitted,

For Applicants

MN:cgm

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Version with markings to show changes made:

Claim 16 (amended). A method of fabricating a semiconductor configuration, which comprises the following steps:

fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;

[introducing] placing a passivating substance X into the monocrystalline silicon layer, during or after the fabrication of the semiconductor structure; and

heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X in the monocrystalline silicon layer to diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.

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